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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,302	12/21/2000	Rajiv Bhatnagar	22109.0012U1	1835

23859 7590 04/08/2003

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EXAMINER
BARNES, CRYSTAL J

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 04/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,302	BHATNAGAR, RAJIV	
	Examiner	Art Unit	
	Crystal J. Barnes	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show "the Configurable Logic Circuit 25 receives signals 15a-15h from the Load Interface Unit 12 and sends signal 14 to it" (see page 15 lines 20-22), "the Analog-to-Digital converter 38 receives the data for the sensitivity and offset correction from the Non-Volatile Memory M" (see page 16 lines 14-16), "the Analog-to-Digital converter 45 receives the data for the sensitivity and offset correction from the Non-Volatile Memory M" (see page 17 lines 7-9), "the sensitivity and offset correction data M are received..." (see page 20 lines 11-15), "...using data M..." (see page 21 lines 4-7), "...signals M..." (see page 21 lines 17-20) as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the

Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because reference number "16" in figure 6 should be reference number "12" (see page 21 line 23). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "cover open sensor 60" on page 23 lines 18 is not shown in figure 4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the

description: reference numbers "13a-13h" in figures 1, 2; reference numbers "27, 29, 34, 35" in figure 3; reference number "64" in figure 4; reference number "7a" in figure 5; and reference number "24" in figure 8 do not appear in the specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities: "input data 8a-8b" on page 14 line 24, page 15 line 19 should be "input data 8a-8f" as shown in figures 1-3; "signals 15a-15f" on page 15 lines 4-5 should be "signals 15a-15p" as shown in figures 1-3; "outputs 5a-5d" should be "outputs 5a-5f" as shown in figures 1-3; "User Interface" on page 16 line 7 should be "Input Interface" as shown in figure 4; "signal 8f" on page 17 line 17, page 21 line 15 should be "signal 8e" as shown in figure 5; "output 14g" on page 18 line 13 should be "output 14" as shown in figure 6; "Figure 8" on page 23 line 6 should be "Figure 9"; on pages 23-24, lines 22-18 are shown in figure 5 not figures 4 or 9; on page 24, lines 18-22 are

shown in figure 3 not figures 4 or 9 and lines 22-25 are shown in figure 6 not figure 4; "latches 52a-52e and drive switches 53a-53e" on page 24 lines 24-25 should be "latches 52a-52f and drive switches 53a-53f" as shown in figure 6. Appropriate correction is required.

7. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

8. Claim 2 is objected to because of the following informalities: "he" should be "the" (see page 27 line 4) and no fourth output is recited in the claim before the fifth output (see page 28 line 3) and sixth output (see page 28 line 13). Appropriate correction is required.

9. Claims 8-11 objected to because of the following informalities: a Configurable Logic Circuit is recited in claim 2 not claim 1. Claims 8-11 should depend from claim 2. Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 8-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claims 8-11 recite the limitation "the said Configurable Logic Unit" in the second line of the claims. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-6, 8, 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 4,245,309 to Kiefer in view of USPN 3,819,906 to Gould, Jr.

As per claim 1 wherein a configurable electronic controller appliances comprising a Non-Volatile Memory [on-board ROM], a configurable Central Control Unit [microprocessor], one set of inputs of the said Central Control Unit [microprocessor] are connected to the outputs of an Input Interface Unit [input scanning 56], one set of outputs of the said Central Control Unit [microprocessor] are fed back to the said Input Interface Unit [input scanning 56], a second set of inputs of the said Central Control Unit [microprocessor] receive user input data from the outputs of a User Interface Unit [control panel switches 58, control panel display 68], a second set of outputs of the said Central Control Unit [microprocessor] are fed back to the said User Interface Unit [control panel switches 58, control panel display 68], a third input of the said Central Control Unit [microprocessor] is connected to one output of a Load Interface Unit [relay drivers 67], a third set of outputs from the said Central Control Unit

[microprocessor] are connected to the inputs of the said Load Interface Unit [relay drivers 67], a fourth input of the said Central Control Unit [microprocessor] receives power supply condition signals from a Supply Interface Unit [DC power supply 130], the said Non-Volatile Memory Unit [on-board ROM] provides non-volatile storage of data and is connected to main circuit blocks consisting of the said Central Control Unit [microprocessor], Input Interface Unit [input scanning 56], User Interface Unit [control panel switches 58, control panel display 68], Load Interface Unit [relay drivers 67], and Supply Interface Unit [DC power supply 130], the output of a Clock Generator circuit [zero crossing detector 66] is connected to one input of each of the said main circuit blocks and produces a clock signal required for their operation, the output of a Reset circuit [zero crossing detector 66] is connected to one input of each of the said main circuit blocks and produces a reset signal required for their proper initialization, the arrangement between the components of the main circuit blocks is such that the said Central Control Unit [microprocessor] receives sensed parameter data supplied by the various sensing devices [relays] in the appliance [consumer appliances], from the said Input Interface Unit [input scanning 56], user requirement data from the said User Interface Unit [control panel switches 58, control panel display 68], load

conditions data from the said Load Interface Unit [relay drivers 67], and the supply conditions data from the said Supply Interface Unit [DC power supply 130], and processes all this data in accordance with its configured functionality and then applies signals to the inputs of the said Load Interface Unit [relay drivers 67] for operating the actuating devices [motors, solenoids] in the appliance for controlling its operation, and to the inputs of the said User Interface Unit [control panel switches 58, control panel display 68] for providing feedback to the user; the Kiefer reference discloses five sources of inputs which are monitored by the microprocessor may be summarized as: inputs from the control panel 58, the door interlock 52, the flood switch 60, the drain feedback 62, and a zero crossing detector 66 used for generating external interrupts in the microprocessor (see figure 1 and column 3 lines 33-38). Responsive to these inputs and based on the control program stored in the microprocessor; three types of output functions are performed: the microprocessor provides power control by activating selected ones of the relays 50 through relay drivers 67, it updates a control panel display 68 via an output scanning matrix 70, and it drives an audio transducer to provide audio feedback during cycle selection by the user (see column 3 lines 38-46). The relays 50 controlled by the microprocessor close circuits to a drain solenoid 74, a pump

motor 76, heater 78, and a water valve solenoid 80, each relay in set 50 being uniquely associated with one of these circuits (see column 3 lines 47-51).

As per claim 2 wherein the said Central Control Unit [microprocessor] consists of a Configurable Logic Circuit [firmware] for implementing the basic control algorithms [control program] that determine the functioning of the appliance [appliance], which is configured for the required functionality by the configuration data supplied by the said Non-Volatile Memory [on-board ROM], one set of inputs of the said Configurable Logic Circuit [firmware] are connected to the outputs of the said Input Interface Unit [input scanning 56] for receiving the signals from various sensing elements in the appliance, one set of outputs of the said Configurable Logic Circuit [firmware] is connected to the input of the said Input Interface Unit [input scanning 56] for controlling its internal operation, a second set of inputs of the said Configurable Logic Circuit [firmware] is connected to one output of the said User Interface Unit [control panel switches 58, control panel display 68] for receiving user supplied data, a second set of outputs of the said Configurable Logic Circuit [firmware] is connected to the input of the said User Interface Unit [control panel switches 58, control panel display 68] for supplying feedback to the user as well as for controlling the internal operation of

the said User Interface Unit [control panel switches 58, control panel display 68], a third input of the said Configurable Logic Circuit [firmware] is connected to one output of the said Load Interface Unit [relay drivers 67] for receiving data about the load conditions, a third set of outputs of the said Configurable Logic Circuit [firmware] is connected to one input of the said Load Interface Unit [relay drivers 67] for controlling the load as well as for controlling the internal operation of the said Load Interface Unit, a fourth input of the said Configurable Logic Circuit [firmware] is connected to one output of the said Supply Interface [power supply 130] for receiving data on the supply conditions, a fifth input of the said Configurable Logic Circuit [firmware] is connected to a Counters and timers block which contains an array of counters and timers required for the operation of the appliance, a sixth input of the said Configurable Logic Circuit [firmware] is connected to a memory circuit for reading of data stored therein, a fifth output of the said Configurable Logic Circuit [firmware] is connected to the said memory circuit for writing data into it, a seventh input of the said Configurable Logic Circuit [firmware] is connected to the output of a Sequence Control circuit which provides the control signals required for defining the sequence of operations performed by the said Configurable Logic Circuit [firmware], an eighth input of the

said Configurable Logic Circuit [firmware] is connected to a Real-Time-Clock (RTC) circuit which provides time-of-day information required for the functioning of the Configurable Logic Circuit [firmware], a sixth output of the said Configurable Logic Circuit [firmware] is connected to the input of the said RTC circuit for setting its value when required, the arrangement between the said Configurable Logic Circuit [firmware], Sequence Control circuit, Counters and Tuners block, Memory block, and RTC circuit is such that the sensor data received from the said Input Interface Unit [input scanning 56], user requirement data received from the said User Interface Unit [control panel switches 58, control panel display 68], load conditions data supplied by the said Load Interface Unit [relay drivers 67], and supply conditions data furnished by the said Supply Interface Unit [power supply 130], are processed by the said Configurable Logic Circuit [firmware] under the control of signals from the said Sequence Control circuit, using data supplied by the said Memory block, said Counters and Timers block and said RTC circuit, to generate the outputs required to control the loads through the said Load Interface Unit [relay drivers 67], provide feedback data required for the user through the said User Interface unit [control panel switches 58, control panel display 68], as well as supply signals required to update the data stored in the said

Memory block, said Counters and Timers block and said RTC circuit, for use in subsequent processing; the Kiefer reference discloses the microprocessor utilized is in a single chip device including an on board ROM in which the control program is permanently installed prior to shipment of the appliance to the user (see column 8 lines 37-41). It is possible to make changes by substituting a new chip containing a revised program and thus field modification of the appliance to add additional options (see column 8 lines 59-62). The base level program includes a number of software routines including the cancel-drain routine 198, a main routine 200, execution routine 202, and cycle interruption routine 204 (see figure 13 and column 9 lines 1-6). The on board ROM contains instructions for effecting the logical steps each time power is applied to the control circuit or a reset is desired (see figure 14 and column 9 lines 44-51). The main routine is entered by any of the other routines upon completion or branching from such other routines (see figure 13 and column 9 lines 64-66). The microprocessor's internal timers are cleared and the stack pointer initialized (see figures 16, 16A and column 10 lines 14-19). The microprocessor based control circuit is capable of initiating a drain operation and then monitoring that operation on a real time basis to detect various malfunctions of the drain system (see figure 17 and column 10 lines 55-58). The current status

of the relay drivers is also output by the external interrupt routine (see figure 18 and column 11 lines 32-33). After saving data, control is transferred to SCN sub-routines 1 through 8, which performs all of the I/O for updating the panel display and inputting selections from membrane switches which may have been pushed (see figure 19 and column 11 lines 39-45). The cancel-drain routine interrupts normal machine action (see figure 20, 20A and column 11 lines 65-66). The door monitor routine is used to suspend operation of the appliance and disable the cycle timer whenever the door is open (see figure 21A and column 12 lines 22-24). The flood protection routine functions to pump out water in the machine whenever an overfill condition is recognized by the flood switch (see figure 21B and column 12 lines 32-35). The flood routine can be activated during machine operation or when the machine is off since the microprocessor remains on regardless of the state of the appliance (see column 12 lines 42-45).

As per claim 3 wherein the said Input Interface Unit [input scanning 56] consists of Sensor Drive circuits for providing bias signals to external sensing devices connected to the Electronic Appliance Controller, the output of each of the said Sensor Drive circuit is connected to the input of one channel of an Analog Multiplexer, the output of the said Analog Multiplexer is connected to the input of

an Analog-to-Digital Converter, the said Analog-to-Digital Converter contains in-built circuitry for the correction for the sensitivity and offset of the signal from each sensing device, the output of the said Analog-to-Digital converter is connected to one input of a Digital Comparator, the other input of the said Digital Comparator is connected to the said Central Control Unit for receiving a reference signal, the output of the said Digital Comparator is connected to one input of a Digital Multiplexer, the other inputs of the said Digital Multiplexer receive digital signals from various sensing devices in the appliance, the output of the said Digital Multiplexer is connected to the input of a Noise Filter, the output of the said Noise Filter is connected to an input of the said Central Control Unit for furnishing data on the signals received from the various sensing devices, a Digital Demultiplexer receives input signals from the said Central Control unit and produces multiple digital output signals for scanning the status of various digital sensing devices in the appliance, the arrangement between the said Analog Multiplexer, said Analog-to-Digital Converter, said Digital Comparator, said Digital Multiplexer, and said Noise Filter is such that the sensor data received from analog sensors is selected by the said Analog Multiplexer Circuit under the control of signals from the said Central Control Unit, converted to digital form by the said

Analog-to-Digital converter and applied to the inputs of the said Digital Multiplexer which also receives other digital signals directly from digital sensing devices in the appliance which are scanned by signals supplied by the said Digital Demultiplexer using signals supplied by the said Central Control Unit, and then applies these one-at-a-time under control of signals from the said Central Control Unit, to the input of the said Noise Filter for filtering and supplying to the said Central Control Unit for processing; the Kiefer reference discloses a mechanical latch 132 controls operation switch 52. By means of an optoisolator 54 the door switch status is communicated to the microprocessor 64 which then de-energizes the switching contacts of relays (see figure 5 and column 37-43). When switch 60 opens it provides an input via the optoisolator 54 to the microprocessor either through the input matrix 56 or directly to the microprocessor through an available I/O port (see figures 7, 8 and column 6 lines 17-21). When the drain solenoid 74 is operated, the drain feedback switch 62 is closed thereby providing an input to the microprocessor 64 via optoisolator 54 (see figures 9, 10 and column 6 lines 31-40).

As per claim 4 wherein the said User Interface Unit [control panel switches 58, control panel display 68] consists of Sensor Drive circuits for providing bias signals to various analog components, such as potentiometers, used for obtaining

user selection values, the output of each of the said Sensor Drive circuits is connected to the input of one channel of an Analog Multiplexer, the output of the said Analog Multiplexer is connected to the input of an Analog-to-Digital Converter, the said Analog-to-Digital Converter contains circuitry for providing in-built correction to the sensitivity and offset of the signal from each sensing device, the output of the said Analog-to-Digital converter is connected to one input of a Digital Comparator, the other input of the said Digital Comparator is a reference signal received by the User Interface Unit from the Central Control Unit, the output of the said Digital Comparator is connected to one input of a Digital Multiplexer, the other inputs of the said Digital Multiplexer receive digital signals from various front-panel switches provided for receiving user input, the output of the said Digital Multiplexer is connected to the input of a Noise Filter, the output of the said Noise Filter is connected to an input of the said Central Control Unit, a Digital Demultiplexer receives input signals from the said Central Control unit and produces multiple digital output signals for scanning the status of the various digital inputs, such as switches, for obtaining user input, a second set of signals from the said Central Control Unit are connected to a set of Latches, the output of each of the said Latches is connected to the input of a Display and

Audio Driver circuit which contains the circuitry for driving the display device and audio output device for providing output data to the user, the arrangement between the said Analog Multiplexer, said Analog-to-Digital Converter, said Digital Comparator, said Digital Multiplexer, said Noise Filter, said Digital Demultiplexer, and said Display and Audio Driver circuits is such that the sensor data received from the analog sensors in the User Interface is selected by the said Analog Multiplexer Circuit under the control of signals from the said Central Control Unit, converted to digital form by the said Analog-to-Digital converter and applied to the inputs of the said Digital Multiplexer which also receives other digital signals received directly from digital sensing devices in the User Interface which are scanned by signals supplied by the said Digital Demultiplexer using signals from the Central Control Unit, and selectively applies them to the said Noise Filter under control of the said Central Control Unit, for filtering and supplying to the said Central Control Unit for processing, while simultaneously the said Display and Audio Driver circuit drives the external display and audio output devices in accordance with the data supplied by the said Central Control Unit; the Kiefer reference discloses a user control panel is illustrated containing the control panel switches and displays by which the user can interface with the control circuit and the

controlled application (see figure 2 and column 4 lines 15-18). When a membrane switch 90 has been touched and the input received and accepted by the microprocessor, an output is produced illuminating the appropriate LED 92 to confirm to the user that the control circuit has accepted a desired cycle option (see column 4 lines 27-32). The seven-segment display is updated by the microprocessor and always displays either the time to the end of the cycle or one of the diagnostic codes (see column 4 lines 37-39). The membrane-multiplexed switches on the control panel are connected in a switch matrix 110 for communication with the microprocessor (see figure 4 and column 4 lines 59-61). Each row of the matrix 110 is connected as an input to the microprocessor 64 (see column 5 lines 13-20). When the cancel switch is closed an external reset of the microprocessor is performed causing interruption of the cycles in process, draining of water in the appliance and a reset of the microprocessor occurs (see column 5 lines 24-30).

As per claim 5 wherein the said Load Interface Unit [relay drivers 67] consists of a plurality of Latches for storing the data received from the said Central Control Unit [microprocessor], the output of each of the said Latches is connected to the input of a Switch Control circuit, the output of each of the said

Switch Control circuits drives a Switch that operates a Load which is an actuating device in the appliance used to control its operation, one end of each of the said Switches is connected to the Load while the other end of the Switch is connected to a Current Sensor for sensing the current through the load, the output from each of the said Current Sensors is connected to one input of an Analog Multiplexer, the output of the said Analog Multiplexer is connected to the input of a Load Sense Circuit which incorporates in-built correction for the sensitivity and offset of the signal from each Shunt, the output of the said Load Sense Circuit is connected to one input of a Digital Comparator, the other input of the said Digital Comparator is a reference signal received by the said Load Interface Unit from the Central Control Unit, the output of the said Digital Comparator is connected to an input of the said Central Control Unit, the arrangement between the said Latches, said Switch Drive Circuits, said Switches, said Current Sensors, said Analog Multiplexer, said Load Current Sensing Circuit, said Digital Comparator and said output Latch, is such that the load current data received by the said Load Current Sensors is converted to digital form by the said Load Current Sense Circuit, compared with reference data supplied from the said Central Control Unit by the said Digital Comparator and supplied to the said Central Control Unit which

furnishes signals for controlling the operation of the said Switch Drive Circuits through the said Latches; the Kiefer reference discloses the three columns are outputs from the microprocessor applied to the matrix via a BCD to decimal decoder 112 (see figure 4 and column 5 lines 14-16). When the door switch is closed, power is applied to the relays permitting their selective actuation by the microprocessor through drivers 67 (see figure 5 and column 5 lines 53-55). When the flood switch opens it interrupts the circuit path from the associated relay 50 to the water solenoid 80 and immediately shuts off the water supply to the appliance (see figure 7 and column 6 lines 13-17). The flood control routine discontinues normal operation of the appliance and initiates a drain cycle which persists until flood switch 60 returns to its normally closed position indicating a safe water level in the appliance (see column 6 lines 24-28). The drain solenoid 74 is actuated by the associated relay 50 in order to initiate draining of water from the appliance (see figures 9, 10 and column 34-36).

As per claim 6 wherein the said Supply Interface Unit [power supply 130] consists of a Supply Voltage Sense circuit which senses the voltage level of the input supply voltage, the output of the said Supply Voltage Sense circuit is connected to one input of each of two digital comparators, the second input of

each of the said Digital Comparators is connected to a signal received from the said Central Control Unit [microprocessor], the outputs of the said Digital Comparators are connected to the input of a Latch, the output of the said Latch, is connected to an input of the said Central Control Unit [microprocessor], the arrangement between the said Supply Voltage Sense circuit, said Digital Comparators, and said Latch is such that the sensed supply voltage is converted to digital form by the said Supply Voltage Sense circuit and compared by the said Digital Comparators with reference data supplied by the said Non-Volatile Memory, and the results of the comparison are latched by the said Latch and furnished to the said Central Control Unit [power supply 130] as supply condition data; the Kiefer reference discloses rectifier 142 produces a 24 volt DC power output for driving the relay coils. Rectifier 143 provides an output to a three terminal regulator 145 producing a five-volt DC power supply for the microprocessor. Rectifier 143 also produces a 12-volt DC supply for the audio and reset circuits. Rectifier 144 produces 24 volts DC for the timing circuit 66. (See figure 6 and column 5 lines 58-68).

As per claim 9 wherein the said Configurable Logic Unit [microprocessor] in another implementation is an embedded in micro programmed controller that is

configured by the configuration data supplied by the said Non-Volatile Memory, the Kiefer reference discloses the microprocessor utilized is in a single chip device including an on board ROM in which the control program is permanently installed prior to shipment of the appliance to the user (see column 8 lines 37-41). It is possible to make changes by substituting a new chip containing a revised program and thus field modification of the appliance to add additional options (see column 8 lines 59-62).

The Kiefer reference does not expressly disclose the arrangement of the main blocks of the present invention.

The Gould, Jr. reference discloses a range incorporating digital control and display panel means (see column 1 lines 3-5). The panel 16 provides control information to a digital logic system 28 which controls the application of power to the various range heating elements 30 and also provides display information to the panel 16 (see figure 2 and column 2 lines 31-36). The instruction address pads 44 corresponding to the various instructions which may be entered from the display panel 16 are connected with an encoder 46 which generates a binary coded decimal instruction which is stored in an instruction latch 48 (see figure 4 and column 3 lines 20-26). The data stored in the latch 82 is converted to analog data by a D/A

converter 86 and is compared in a comparator 88 with the output of a temperature sensor 90 located in the oven (see column 4 lines 10-14 19-23). More detailed logic diagrams are shown in figures 5-15 (see column 4 lines 59-66).

As per claim 8 wherein the said Configurable Logic Unit [firmware] in one implementation is a Gate Array that is configured by the configuration data supplied by the said Non-Volatile Memory; the Gould, Jr. reference disclose the gating 122 also receives inputs from the OFF address pad and clock generator 52 (see figure 5 column 5 lines 23-25). A memory one-shot 222 is triggered from the digit one-shot 120 through the gating 220 to enable the WRITE ENABLE input to the memory elements 72a-72d so that the data from the shift register 78 may be written into memory (see figure 7 and column 7 lines 47-51). The gating 220 further includes an AND gate 254 and an OR gate 256 which causes the memory one-shot 222 to be triggered each time the digit one-shot 106 is triggered unless a surface unit address pad has been touched (see columns 8-9 lines 55-60, 65-2). During the CLEAN cycle the characters EC are displayed on the displays 76b and 76c. This is accomplished by a latch 384 and gating 386 and 388 interconnected between the memory elements 72b and 72c and decode driver 74b, 74c (see figure 11 and columns 14-15 lines 66-6).

As per claim 12 wherein the said Clock Generator is an oscillator with a frequency preferably in the range 32 KHz to 25 MHz, the Gould, Jr. reference discloses the circuitry includes an oscillator 600 producing square wave outputs of, for example, 100 KHz (see figure 17 and column 20 lines 8-9).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the microprocessor based control circuit taught by the Kiefer reference with the control circuit taught by the Gould, Jr. reference to illustrate the arrangement of the essential elements of a microprocessor to support various inputs/outputs. The arrangement of essential elements of a microprocessor is a modification that has been considered to be within the level of ordinary skill in the art.

One of ordinary skill in the art would have been motivated to utilize any desired arrangement to support various inputs/outputs of a microprocessor as long as central control was provided for the desired application. Most applications utilizing central/master processors require inputs interfaces to acquire data and permit operator inputs and output interfaces to control actuators and display information to the operator. Depending on the application, more or less I/O interfaces may be needed.

15. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 4,245,309 to Kiefer in view of USPN 5,621,662 to Humphries et al.

As per claim 7 wherein it further includes a Network Interface Unit [host interface 24] that is connected to another output from the said Central Control Unit [microprocessor] and provides an input to the said Central Control Unit [microprocessor] for exchanging data between an external network [host computer 20] and the said Central Control Unit [microprocessor]; the Kiefer reference does not expressly disclose a Network Interface Unit.

The Humphries et al. reference discloses the network comprises a host computer 20 connected through a host interface 24 to a plurality of nodes (see figure 3 and column 6 lines 39-41). The host interface 24 comprises a bus interface circuit 40, a neuron processor circuit 42, and an opto-isolation circuit 44 (see figure 4 and column 6 lines 59-61).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to include the appliance control taught by the Kiefer reference within the home automation system taught by the Humphries et al.

reference to illustrate another hardware device connected to the node as an appliance (see Humphries 45-47).

One of ordinary skill in the art would have been motivated to modify the home automation system to include the appliance to expand the capability of the home automation system by including more complex hardware devices.

16. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 4,245,309 to Kiefer in view of USPN 6,320,286 to Ramarathnam.

As per claim 10 wherein the said Configurable Logic Unit [firmware] in another implementation is configurable for providing over current protection [over-current protection means] and "Soft Start" facility [soft start means] that supplies a reduced voltage start to the load in order to minimize in-rush current stress at turn-on, selectively to the loads through the signals applied to the inputs of the said Load Interface Unit [relay drivers]; the Kiefer reference does not expressly disclose providing over current protection and "Soft Start" facility.

As per claim 11 wherein the said Configurable Logic Unit [firmware] in another implementation is configurable for providing overheat protection [thermal overload protection means] selectively to the loads using temperature data

supplied by sensing devices physically attached to the selected loads through the signals supplied by the said Input Interface Unit [input scanning], and supplying applying signals to the inputs of the said Load Interface Unit [relay drivers] to turn-off the drive to the loads in case of overheat conditions; the Kiefer reference does not expressly disclose providing overheat protection.

The Ramarathnam reference discloses the controller is a microcontroller with the associated processor, ROM, RAM and the I/O ports having the software program in ROM to produce timing signals through the output port to the gates through the driver IC. The software program includes soft-start means. (See column 4 lines 33-38). Thermal over-load protection means is provided for the motor windings. The over-current protection means is provided for the PWM bridge inverter. (See column 4 lines 48-51). There is also an over-current protection for the bridge and whenever this set is exceeded the bridge is completely shut off by the controller (see column 8 lines 21-23). When the tool is switched ON, the controller does not set the voltage and the frequency corresponding to the rated values (see column 8 lines 28). The inrush current during the acceleration is kept within the desired limits (see column 8 lines 63-67).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the firmware taught by the Kiefer reference with the software taught by Ramarathnam reference to incorporate various protection means specific to certain applications.

One of ordinary skill in the art would have been motivated to modify the firmware of the microprocessor based control circuit to include additional software to provide a configurable microprocessor based control circuit solely depended on the firmware/software installed in the ROM of the control circuit.

17. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 4,245,309 to Kiefer in view of USPN 6,006,996 to Bhatnagar.

As per claim 10 wherein the said Configurable Logic Unit [firmware] in another implementation is configurable for providing over current protection [over-current protection circuit] and "Soft Start" facility ["Soft Start" circuit] that supplies a reduced voltage start [reduced voltage start-up] to the load [load] in order to minimize in-rush current [in-rush current] stress at turn-on [turn-on], selectively to the loads through the signals applied to the inputs of the said Load

Interface Unit [relay drivers]; the Kiefer reference does not expressly disclose providing over current protection and "Soft Start" facility.

As per claim 11 wherein the said Configurable Logic Unit [firmware] in another implementation is configurable for providing overheat protection [thermal overload protection] selectively to the loads using temperature data supplied by sensing devices physically attached to the selected loads through the signals supplied by the said Input Interface Unit [input scanning], and supplying applying signals to the inputs of the said Load Interface Unit [relay drivers] to turn-off the drive to the loads in case of overheat conditions; the Kiefer reference does not expressly disclose providing overheat protection.

The Bhatnagar reference discloses the output drive and protection circuit (10) which includes the 'Soft Start' circuit (10A), thermal over-load protection circuit (10B) and over-current protection circuit (10C) drives the Solid State Switch (11) to actuate the relevant device in the consumer/industrial appliance to correct the temperature and minimize the in-rush current stress produced on the load in case of motor and heater loads as well as protect against over-heat and current over-load conditions (see figures 1, 1a and column 6 lines 46-54). The outputs from the output drive and protection circuits (46) to (50) connect to the

inputs of solid state switches (51) to (55) through the said output drive and protection circuits which drive and monitor the load (blower, compressor, heater, pump or solenoid valve of the refrigeration/heating system). Any one or more of the output drive and protection circuits (46) include a `Soft Start` Circuit (46A), thermal over-load protection circuit (46B) and over-current protection circuit (46C) to provide an effective reduced voltage start-up to the load, during the initial period of turn-on and thereby decrease the in-rush current stress produced on the load in case of motor and heater loads and protection against thermal and current over-load conditions (see figures 8, 8a and column 9 lines 14-27).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the microprocessor based control circuit taught by the Kiefer reference with the control unit taught by Bhatnagar reference to incorporate various protection means specific to certain applications.

One of ordinary skill in the art would have been motivated to modify the microprocessor based control circuit with the control unit to illustrate that the applicability of the microprocessor based control circuit solely depended on the firmware/software installed in the ROM of the control circuit.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to central control systems in general:

USPN 6,460,565 B1 to Titus

USPN 6,449,515 B2 to Imoto

USPN 6,285,912 B1 to Ellison et al.

USPN 6,249,711 B1 to Aart

The following patents are cited to further show the state of the art with respect to control system interfaces in general:

US Pub. No. 2003/0040812 A1 to Gonzales et al.

USPN 5,225,974 to Mathews et al.

USPN 4,570,215 to Miura et al.

The following patents are cited to further show the state of the art with respect to control circuits with protection means in general:

USPN 6,263,839 B1 to Hoshiba et al.

USPN 5,898,557 to Baba et al.

USPN 5,648,008 to Barritt et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Crystal J. Barnes whose telephone number is 703.306.5448. The examiner can normally be reached on Monday-Friday alternate Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A. Follansbee can be reached on 703.305.8498. The fax phone numbers for the organization where this application or proceeding is assigned are 703.746.7239 for regular communications and 703.746.7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.305.3900.

cjb
April 5, 2003

EMANUEL TODD VOELTZ
PRIMARY EXAMINER